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DEPARTMENT OF HIGHER EDUCATION AND TRAINING
REPUBLIC OF SOUTH AFRICA
NATIONAL CERTIFICATE
LOGIC SYSTEMS N3
TIME: 3 HOURS
MARKS: 100

INSTRUCTIONS AND INFORMATION

1. Answer ALL the questions.
2. Read ALL the questions carefully.
3. Number the answers according to the numbering system used in this question paper.
4. ALL the sketches and diagrams must be large, clear and neat.
5. Keep questions and subsections of questions together.
6. Show ALL the steps and calculations.
7. Write neatly and legibly.
QUESTION 1: NUMBER SYSTEMS AND ARITHMETIC ELEMENTS

1.1 If X = 64_{16}, Y = 24_{8} and Z = 15_{10}, calculate the following:

1.1.1 The value of X in the octal number system (2)
1.1.2 The product of Y and Z in the binary number system (4)
1.1.3 X divided by Y in the binary number system (3)
1.1.4 Use 2's complement to subtract 144_{8} from X. (4)

1.2 Complete the following TRUTH TABLE by filling in the missing binary digits. Write only the answer next to the question number (1.2.1–1.2.5) in the ANSWER BOOK.

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

TABLE 1 (5)

1.3 Briefly describe a half-adder. (2)

QUESTION 2: CODES, DATA AND DATA COMMUNICATION, ENCODERS AND DECODERS

2.1 Give an example of each of the following codes:

2.1.1 Self-complementing weighted code
2.1.2 Non-weighted code (2 × 1) (2)

2.2 What does ASCII stand for? (2)

2.3 Give ONE function of an encoder. (2)
2.4  Convert the following numbers to the indicated code:

2.4.1  $11101001101_{2421BCD}$ code to decimal

2.4.2  $103_{10}$ to XS3 (excess 3) code  \((2 \times 3)\)  \((6)\)

2.5  The following word is received at the end of a transmission data line:

```
1 0 1 1 1 0 1 1
1 0 0 0 1 0 1 1
1 1 1 0 0 1 0 0
1 0 1 0 1 1 0 0
1 0 0 0 1 1 1 1
1 1 1 1 1 1 1 1
```

By using even parities, determine whether any faults occurred during transmission and if so, rectify the fault(s).  \((8)\)  \([20]\)

**QUESTION 3: LOGIC GATES, INTEGRATED CIRCUITS AND LOGIC FAMILIES**

3.1  One way to think of logic gate types is to consider what input states guarantee a certain output state.

For example, an AND gate could be described as the function whereby any LOW input guarantees a LOW output.

Identify what type of gate is represented by each of the following statements:

3.1.1  Any LOW input guarantees a HIGH output.

3.1.2  Any difference in the input guarantees a LOW output.

3.1.3  Any HIGH input guarantees a HIGH output.  \((3 \times 2)\)  \((6)\)

3.2  Show, by means of a circuit diagram, how diodes can be used to construct an OR gate.  \((5)\)
3.3 Study FIGURE 1 below and answer the questions.

3.3.1 Copy the TRUTH TABLE below in your ANSWER BOOK and use FIGURE 1 above to complete it.

<table>
<thead>
<tr>
<th>INPUTS</th>
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<tr>
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<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

3.3.2 What type of logic gate is represented by output Z in FIGURE 1?

3.3.3 Draw the IEC symbol for the logic gate identified in QUESTION 3.3.2.

3.4 What is the minimum number of inputs that an AND gate can have?
QUESTION 4: MEMORY ELEMENTS AND MEMORIES

4.1 Choose an answer from COLUMN B that matches a description in COLUMN A. Write only the letter (A–G) next to the question number (4.1.1–4.1.5) in the ANSWER BOOK.

<table>
<thead>
<tr>
<th>COLUMN A</th>
<th>COLUMN B</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1.1 Time required to change the voltage level from 90% to 10%</td>
<td>A  edge triggering</td>
</tr>
<tr>
<td>4.1.2 Minimum time the data signal should be held steady before the clock event, so that the data is reliably sampled by the clock</td>
<td>B  rising time</td>
</tr>
<tr>
<td>4.1.3 A flip-flop triggered by either the positive edge or negative edge of the clock pulse</td>
<td>C  holding time</td>
</tr>
<tr>
<td>4.1.4 Time required to change the voltage level from 10% to 90%</td>
<td>D  falling time</td>
</tr>
<tr>
<td>4.1.5 Minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop</td>
<td>E  level triggering</td>
</tr>
<tr>
<td></td>
<td>F  delay time</td>
</tr>
<tr>
<td></td>
<td>G  setup time</td>
</tr>
</tbody>
</table>

4.2 Briefly explain the difference between a combinational- and a sequential circuit.

4.3 Study FIGURE 2 below and then answer the questions.

FIGURE 2

4.3.1 When a 1 is applied to both the set (S) and reset (R) inputs of the flip-flop in FIGURE 2 above the outputs are termed to be invalid.

Why are the outputs invalid?  

4.3.2 Draw the IEC symbol for the flip-flop in FIGURE 2.
4.4 Draw a labelled single-cell structure for a dynamic read-write memory (DRAM).  

(5)

4.5 An SRAM cell has three different operating states of which one is standby. 

Name the remaining TWO modes of operation.  

(2)  

[20]

QUESTION 5: SHIFT REGISTERS AND COUNTERS

5.1 Explain the working principle of a 4-bit SISO (series-in-series-out) shift register.  

(12)

5.2 Draw a neat, labelled sketch of 4-bit ring counter making use of a JK flip-flop which is negatively edged.  

(8)  

[20]

TOTAL: 100
MARKING GUIDELINE

NATIONAL CERTIFICATE
APRIL EXAMINATION
LOGIC SYSTEMS N3

5 APRIL 2016

This marking guideline consists of 8 pages.
QUESTION 1

1.1 1.1.1 X = 64_{16} = 01100100_2 \checkmark
= 001 100 100
= 144_8 \checkmark
\therefore Y = 144_8

1.1.2 Y = 24_8 and Z = 15_{10}

<table>
<thead>
<tr>
<th>8</th>
<th>4</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 =</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
\therefore 15_{10} = 1111_2 \checkmark

<table>
<thead>
<tr>
<th>2</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>24_8 =</td>
<td>010</td>
</tr>
</tbody>
</table>
\therefore 24_8 = 10100_2 \checkmark

\[
\begin{array}{cccc}
1 & 0 & 1 & 0 \\
\times & 1 & 1 & 1 & 1 \\
\hline
1 & 0 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 & \checkmark \\
1 & 0 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 \\
\hline
1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & \checkmark \\
\end{array}
\]

1.1.3 X = 64_{16} = 1100100_2

Y = 24_8 = 10100

\[
\begin{array}{cccc}
1 & 0 & 1 & 0 & 0 \\
\hline
1 & 1 & 0 & 0 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 & \downarrow & \downarrow & \checkmark \\
0 & 0 & 1 & 0 & 1 & 0 & \downarrow \\
0 & 1 & 0 & 1 & 0 & 0 & \checkmark \\
\hline
0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \checkmark \\
\end{array}
\]
1.1.4 \( X = 1100100_2 \)

\[
\begin{array}{c|cccc}
1 & 4 & 4 & 144_8 = 001 & 100 & 100 \\
\hline
144_8 & & \downarrow & & & \\
\therefore 144_8 = 1100100_2 & & & \\
\end{array}
\]

2's complement of 1100100 is equal to 0011011 + 1✓ = 0011100✓

\[
\begin{array}{cccccc}
& 1 & \text{carry} & \circ & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\
0 & * & & 0 & 0 & 1 & 1 & 1 & 0 & 0 \\
1 & * & & & & & & & & & \\
\hline
1 & 0 & * & 0 & 0 & 0 & 0 & 0 & 0 & 0 & \\
\end{array}
\]

\( \Rightarrow \) ignore (4)

1.2  
1.2.1  0
1.2.2  1
1.2.3  1
1.2.4  0
1.2.5  1

\( (5 \times 1) \) (5)

1.3 A half-adder is an arithmetic element which has two inputs and two outputs (sum and carry out),✓ and it can add two bits at a time.✓ (2) [20]

**QUESTION 2**

2.1 2.1.1 2421; 4221; 8421; 5211; 3321 or 4321 (Any 1) (1)

2.1.2 Gray or XS3 code (1)

2.2 American Standard Code for Information Interchange (2)

2.3 An encoder is used to convert decimal code to binary or BCD code. (2)

2.4 2.4.1 1 1 1 1 0 1 0 0 1 1 0 1

\[
\begin{array}{cccccc}
\downarrow & 2 & 4 & 2 & 1 & \downarrow & 2 & 4 & 2 & 1 \\
\downarrow & 2 & 4 & 2 & 1 & \downarrow & 2 & 4 & 2 & 1 \\
\downarrow & 9 & 4 & 5 & & & & & & & \\
\end{array}
\]

Copyright reserved
2.4.2

\[
\begin{array}{ccc}
1 & 0 & 3 \\
\downarrow & \downarrow & \downarrow \\
1 & 0 & 3 \\
\frac{+3}{4} & \frac{+3}{3} & \frac{+3}{6} \\
\downarrow & \downarrow & \downarrow \\
0100 & 0011 & 0110
\end{array}
\]

\[(2 \times 3) \quad (6)\]

2.5

\[
\begin{array}{cccc|cc|c|c|c}
1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & e \\
1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 & e \\
1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 & e & \checkmark \\
1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & e \\
\hline
1 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & u & \checkmark \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & e & \checkmark \\
e & e & e & e & u & e & e & e & \checkmark \\
\hline & & & & & & & & & \\
\checkmark & \checkmark & \checkmark & & & & & & & \\
\end{array}
\]

The fault is in column 5, row 5, the 1 (one) is changed to a 0 (zero)

\[
\begin{array}{cccc|cc|c|c|c}
1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 \\
1 & 0 & 0 & 0 & 1 & 0 & 1 & 1 \\
1 & 1 & 1 & 0 & 0 & 1 & 0 & 0 \\
1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 & \checkmark & \checkmark & 1 & 1 & 1 \\
1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\
\end{array}
\]

\[(8) \quad [20]\]
QUESTION 3

3.1 3.1.1 NAND gate
3.1.2 XNOR gate
3.1.3 OR gate

(3 × 2) (6)

3.2

A

B

- 

1 mark for direction of diode
1 mark for right connection of diodes
1 mark for resistor
1 mark for output
1 mark for earthing

(5)

3.3 3.3.1

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</tr>
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<td>0</td>
</tr>
</tbody>
</table>

(4)

3.3.2 XOR gate

(1 x 2) (2)

3.3.3

3.4 One (1)

[20]
QUESTION 4

4.1  4.1.1  D  
     4.1.2  G  
     4.1.3  A  
     4.1.4  B  
     4.1.5  C  

(5 x 1)  (5)

4.2  A combinational circuit can be defined as a circuit of which the output is  
dependent only on the inputs at the same instant of time whereas a  
sequential circuit can be defined as a circuit of which the output depends not  
only on the present inputs but also on the past history of inputs.  

(4)

4.3  4.3.1  The outputs are invalid because the outputs of both Q and Q’ go to  
0. This condition violates the fact that the outputs are  
complements of each other.  

(2)

4.3.2

4.4

4.5  • Reading mode  
     • Writing mode  

(2)

[20]
QUESTION 5

5.1 1. Bit 0 is entered into the data input line. $D1 = 0$, first clock pulse is applied, $FF1$ is reset and stores 0.✓
2. Next bit 1 is entered. $Q1 = 0$, since $Q1$ is connected to $D2$, $D2$ becomes 0.✓
3. Second clock pulse is applied, the 1 on the input line is shifted into $FF1$ because $FF1$ sets. The 0 which was stored in $FF1$ is shifted into $FF2$.✓
4. Next bit 0 is entered and third clock pulse applied. 0 is entered into $FF1$, 1 stored in $FF1$ is shifted to $FF2$ and 0 stored in $FF2$ is shifted to $FF3$.✓
5. Last bit 1 is entered and 4th clock pulse applied.✓ 1 is entered into $FF1$, 0 stored in $FF1$ is shifted to $FF2$, ✓ 1 stored in $FF2$ is shifted to $FF3$ and 0 stored in $FF3$ is shifted to $FF4$. This completes the serial entry of 4-bit data into the register. Now the LSB 0 is on the output $Q4$.✓
6. Clock pulse 5 is applied. LSB 0 is shifted out. The next bit 1 appears on $Q4$ output.✓
7. Clock pulse 6 is applied. The 1 on $Q4$ is shifted out and 0 appears on $Q4$ output.✓
8. Clock pulse 7 is applied. 0 on $Q4$ is shifted out. Now 1 appears on $Q4$ output.✓
9. Clock pulse 8 is applied. 1 on $Q4$ is shifted out.✓
10. When the bits are being shifted out (on CLK pulse 5 to 8) more data bits can be entered.✓

5.2

OR
Reset

Shift

TOTAL: 100
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